REMARKS

Claims 5, 7-8, 12-14, 19, 21, and 23 have been amended to remove their multiple dependency. Claim 28 has been cancelled. New claims 29-and 30 are dependent on claim 20. (The amendments to the claims are shown on the attached sheets.) No new matter has been introduced by way of these amendments. Accordingly, with this amendment, twenty-nine claims remain pending.

If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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PATENT
Attorney Docket No. 211178

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael J. UNDERHILL

Art Unit: Unassigned

Corresponding to
Application No. PCT/GB99/03776

Examiner: Unassigned

International Filing Date: November 12, 1999

For: ANTI-JITTER CIRCUITS

CLAIMS AS AMENDED ON MAY 9, 2001

5. (Amended) An anti-jitter circuit [is] as claimed in [any one of the] claim[s] 2 [to 4] wherein said means defining a negative feedback path comprises a low pass filter.

7. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 2 [to 6] wherein said mean d.c. voltage level is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.

8. (Amended) An anti-jitter circuit [is] as claimed in [any one of the] claim[s] 2 [to 7] including a monostable circuit connected to the output of said means for comparing.

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12. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 8 [to 14] wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 1 [to 12] including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

14. (Amended) An anti-jitter circuit as claim in [any one of] claim[s] 1 [to 13] including means for maintaining the charge value of the charge packets substantially constant.

19. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 2 [to 6] wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

21. (Amended) An anti-jitter circuit as claimed in claim 19 [or claim 20] wherein said further negative feedback path comprises a low pass filter.

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23. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 2 [to 6] wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

25. (Amended) An anti-jitter circuit as claimed in [any one of] claim[s] 2 [to 24] including means providing a low impedance path between the input and the output of the negative feedback path.

Cancel claim 28 without prejudice.

29. (New) An anti-jitter circuit as claimed in claim 20 wherein said further negative feedback path comprises a low pass filter.

30. (New) An anti-jitter circuit as claimed in claim 29 wherein said low pass filter comprises the combiantion of a resistor and a capacitor.

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